

**CLAIMS**

What is claimed is:

- 1 1. An interface between a master device and a slave device, said interface comprising a  
2 bit serial bidirectional signal line for conveying commands and associated data from said  
3 master device to said slave device, said bit serial bidirectional signal line further  
4 conveying other signals, said other signals comprising a reset signal, an interrupt signal,  
5 and a learning sequence signal for specifying a duration of a bit time for data transferred  
6 from said slave device to said master device.
- 1 2. An interface as in claim 1, where said master device is comprised of a personal digital  
2 assistant.
- 1 3. An interface as in claim 1, where said master device is comprised of a mobile terminal.
- 1 4. An interface as in claim 3, where said mobile terminal samples the data transferred  
2 from said slave device to said master device at a rate established by a mobile terminal  
3 sleep clock.
- 1 5. An interface as in claim 1, where said interface comprises, in said slave device, an  
2 Accessory Control Interface chip and an oscillator providing a clock signal to said  
3 Accessory Control Interface chip, where the bit time is a multiple of the clock signal, and  
4 where said master device adapts the sampling of the data transferred from said slave  
5 device in accordance with the specified duration of the bit time.
- 1 6. An interface as in claim 1, where said interface comprises, in said slave device, an  
2 Accessory Control Interface chip and a non-volatile memory for storing slave device  
3 related feature data that is readable by said master device over said bit serial bidirectional  
4 signal line in response to a memory read command sent from said master device to said  
5 Accessory Control Interface chip over said bit serial bidirectional signal line.
- 1 7. An interface as in claim 1, where said interface comprises, in said slave device, an

2   Accessory Control Interface chip and a challenge/response authentication function that  
3   is challenged in response to an authentication challenge command and associated  
4   challenge data sent from said master device to said Accessory Control Interface chip over  
5   said bit serial bidirectional signal line, and where authentication result data is sent by said  
6   Accessory Control Interface chip to said master device over said bit serial bidirectional  
7   signal line in response to an authentication result command sent from said master device  
8   to said Accessory Control Interface chip over said bit serial bidirectional signal line.

1   8. An interface as in claim 1, where said bit serial bidirectional signal line further  
2   conveys a slave device connected/disconnected state to said master device.

1   9. An interface circuit for coupling a slave device to a master device, said interface  
2   circuit supporting a bit serial bidirectional signal line that conveys commands and  
3   associated data from said master device to said slave device, said bit serial bidirectional  
4   signal line further conveying other signals, said other signals comprising a reset signal,  
5   an interrupt signal, and a learning sequence signal for specifying a duration of a bit time  
6   for data transferred from said slave device to said master device.

1   10. An interface circuit as in claim 9, where said interface circuit is disposed within said  
2   slave device and comprises an oscillator for generating a clock signal, where the bit time  
3   is a multiple of the clock signal period, and where said master device samples said bit  
4   serial bidirectional signal line in accordance with the specified duration of the bit time.

1   11. An interface circuit as in claim 9, where said interface circuit is disposed within said  
2   slave device and comprises a non-volatile memory for storing slave device related  
3   feature data that is readable by said master device over said bit serial bidirectional signal  
4   line in response to a read command sent from said master device to said interface circuit  
5   over said bit serial bidirectional signal line.

1   12. An interface circuit as in claim 9, where said interface circuit is disposed within said  
2   slave device and comprises a challenge/response authentication function that is  
3   challenged in response to an authentication challenge command and associated challenge  
4   data received from said master device over said bit serial bidirectional signal line, and

5 where authentication result data is sent to said master device over said bit serial  
6 bidirectional signal line in response to receiving an authentication result command from  
7 said master device over said bit serial bidirectional signal line.

1 13. An interface circuit as in claim 9, where said bit serial bidirectional signal line further  
2 conveys a slave device connected/disconnected state to said master device.

1 14. An interface circuit as in claim 9, where said master device is comprised of a mobile  
2 terminal.

1 15. An interface circuit as in claim 14, where said mobile terminal samples said bit serial  
2 bidirectional signal line at a rate established by a mobile terminal sleep clock.

1 16. An interface circuit as in claim 9, where said master device is comprised of a  
2 personal digital assistant.

1 17. An interface circuit for coupling a slave device to a master device, said interface  
2 circuit being disposed in said slave device and supporting a bit serial bidirectional signal  
3 line that conveys commands and associated data from said master device to said slave  
4 device, said bit serial bidirectional signal line further conveying other signals, said other  
5 signals comprising a reset signal.

1 18. An interface circuit as in claim 17, where said other signals further comprise an  
2 interrupt signal and a learning sequence signal for specifying a duration of a bit time for  
3 data transferred from said slave device to said master device.

1 19. An interface circuit for coupling a slave device to a master device, said interface  
2 circuit being disposed in said slave device and supporting a bit serial bidirectional signal  
3 line that conveys commands and associated data from said master device to said slave  
4 device, said bit serial bidirectional signal line further conveying other signals, said other  
5 signals comprising an interrupt signal.

1 20. An interface circuit as in claim 19, where said other signals further comprise a reset

2 signal and a learning sequence signal for specifying a duration of a bit time for data  
3 transferred from said slave device to said master device.

1 21. An interface circuit for coupling a slave device to a master device, said interface  
2 circuit being disposed in said slave device and supporting a bit serial bidirectional signal  
3 line that conveys commands and associated data from said master device to said slave  
4 device, said bit serial bidirectional signal line further conveying other signals, said other  
5 signals comprising a learning sequence signal for specifying a duration of a bit time for  
6 data transferred from said slave device to said master device.

1 22. An interface circuit as in claim 21, where said interface circuit comprises an  
2 oscillator for generating a clock signal, where the duration of the bit time is a multiple  
3 of the clock signal period, and where said master device samples said bit serial  
4 bidirectional signal line in accordance with the specified duration of the bit time.

1 23. An interface circuit as in claim 22, where a logic zero and a logic one are  
2 distinguished by a presence or absence of a transition occurring on said bit serial  
3 bidirectional signal line by a predetermined point in the specified duration of the bit time.

1 24. An interface circuit as in claim 23, where the specified duration of the bit time is  
2 given by  $T$ , and where the predetermined point is about  $T/2$ .

1 25. An interface circuit as in claim 21, where said interface circuit comprises at least one  
2 register that is readable by said master device over said bit serial bidirectional signal line.

1 26. An interface circuit as in claim 21, where said interface circuit comprises at least one  
2 register that is writable by said master device over said bit serial bidirectional signal line.

1 27. An interface circuit as in claim 21, where said interface circuit comprises at least one  
2 memory device location that is readable by said master device over said bit serial  
3 bidirectional signal line.

1 28. An interface circuit as in claim 21, where said interface circuit comprises at least one

2 memory device location that is writable by said master device over said bit serial  
3 bidirectional signal line.

1 29. An interface circuit as in claim 21, where said interface circuit comprises an  
2 authentication block that is addressable by commands sent by said master device over  
3 said bit serial bidirectional signal line, and that responds to at least one command with  
4 response data sent to said master device over said bit serial bidirectional signal line.

1 30. An interface circuit as in claim 21, where said other signals further comprise a reset  
2 signal and an interrupt signal.

1 31. A method for communicating between a master device and a slave device,  
2 comprising:

3 coupling the slave device to the master device through an interface, the interface  
4 comprising a bit serial bidirectional signal line;

5 sending a reset signal from the master device to the slave device over the bit serial  
6 bidirectional signal line;

7 sending a learning sequence signal to the master device over the bit serial bidirectional  
8 signal line for specifying a duration of a bit time for data transferred between the master  
9 device and the slave device; and

10 communicating at least one of data and commands between the master device and the  
11 slave device over the bit serial bidirectional signal line.

1 32. A method as in claim 31, where communicating comprises the master device  
2 sampling the bit serial bidirectional signal line in accordance with the specified duration  
3 of the bit time.

1 33. A method as in claim 32, where a logic zero and a logic one are distinguished by a  
2 presence or absence of a transition occurring on the bit serial bidirectional signal line by

3 a predetermined point in the specified duration of the bit time.

1 34. A method as in claim 33, where the specified duration of the bit time is given by T,  
2 and where the predetermined point is about  $T/2$ .